Ultra Low-Power IoT & AI at the Edge Computing Platform
Optimized For

Edge AI/ML, Security, Smart IoT
ASA Microsystems Inc.

- Founded early 2018
- Capital Efficient Self Funded Operations
- Focused on Ultra Low Power High Performance Technology, IP and Products Optimized for IoT and AI Enabled Edge Computing
- Based in Silicon Valley with R&D office in Japan
- Multiple Customer Driven Product Developed
- Next generation AI Edge Inferencing products in development
- Experienced Management Team with Proven Track Record
Ultra low-power high performance RISC-V based processor and ultra low-power vector-based accelerator to make smart IoT and edge AI computing a cost and time to market practical reality.
Target Markets

- Medical
- Industrial / Robotics
- Building Automation
- Smart Camera / Security
- Smart Appliance
- Smart Sensors
- Smart Drones
- Consumer Products
ASA RISC-V Processors
Why ASA RISC-V Processors

RISC-V:
- An instruction set – independent of processor architecture and implementation
- Commercial RISC-V processors are proprietary implementations of microarchitecture for the common RISC-V instruction set
- Majority RTL generated from chisel-based implementation of RISC-V processor

ASA RISC-V:
- Proprietary patent pending microarchitecture that implements RISC-V ISA in Verilog
- Ultra-efficient in gate count, die size, and power
- Hyper-scaler clock rate
  - Dynamic range from 100’s of megahertz to gigahertz
ASA Processor Core Family Overview (32-bit RISC-V)

<table>
<thead>
<tr>
<th>AR32Z</th>
<th>AR32E</th>
<th>AR128V</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Proprietary micro-architecture.</td>
<td>• Proprietary micro-architecture with parallel execution unit</td>
<td>• Proprietary micro-architecture with vector execution unit as accelerator</td>
</tr>
<tr>
<td>• Core is ready for customer evaluation.</td>
<td>• To deliver highest performance at reasonably lower power consumption.</td>
<td>• High Performance vector operation at lowest power.</td>
</tr>
<tr>
<td>• FPGA development platform ready for prototyping.</td>
<td>• Small footprint</td>
<td>• Proprietary Memory Controller</td>
</tr>
<tr>
<td>• 1/3 of the AR32E footprint</td>
<td>• Lowest power with highest performance (GHz+ at 28nm)</td>
<td>• Applications</td>
</tr>
<tr>
<td>• Applications</td>
<td>• Applications</td>
<td>o AI</td>
</tr>
<tr>
<td>o Sensors interface</td>
<td>o Edge computing</td>
<td>o Vision Processing</td>
</tr>
<tr>
<td>o Energy harvesting</td>
<td>o MPSoC for AI/ML</td>
<td>o Image Processing/DSP</td>
</tr>
<tr>
<td>o Battery operated embedded IoT &amp; Medical applications</td>
<td>o Accelerator coprocessor</td>
<td></td>
</tr>
</tbody>
</table>

M0 – M4

Optional SIMD/MAC/DSP Co-Processor

128-bit Vector Processor

M7 and More
ASA RISC-V Based Technology Portfolio

ARSIM: Complete C/C++ based simulator for verification and software development

Heterogeneous chiplet based system design IP and platform

Multicore processor core system platform

Lowest power RISC-V vector processor

Complete FPGA development and production platform

Software

- Simulator

- Chiplet Ready

- Multi-Core

- Vector Processor

- AI Accelerator Ready

- SoCs

- FPGA

- Tools

Industry’s highest performance with lowest power and smallest size RISC-V processors

Tightly coupled custom AI accelerator integration

Fully verified SoC platform for different applications

Standard software platform and tools for different applications
# Implementation Results in FPGA

Table shows hierarchical implementation result for the AR32Z SoC (reported core part only) using ARTIX-7-100T device at 100MHz operating frequency

<table>
<thead>
<tr>
<th>Name</th>
<th>Slice LUTs</th>
<th>Slice Registers</th>
<th>Slice</th>
<th>LUT as Logic</th>
<th>DSP slices</th>
<th>Dynamic Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ahb_soc</td>
<td>3,502</td>
<td>2,297</td>
<td>1,245</td>
<td>3,454</td>
<td>4</td>
<td>25</td>
</tr>
<tr>
<td>ar32z (ar32z_ahb_top)</td>
<td>1,726</td>
<td>1,005</td>
<td>592</td>
<td>1,678</td>
<td>4</td>
<td>9</td>
</tr>
<tr>
<td>core_inst (core)</td>
<td>1,464</td>
<td>639</td>
<td>478</td>
<td>1,416</td>
<td>4</td>
<td>7</td>
</tr>
</tbody>
</table>
AR32Z vs MicroBlaze in FPGA

FPGA chip: Xilinx Artix-7 100T (speed grade -1)
FPGA Board: Nexys A7
Operating Clock Frequency: 100MHz

<table>
<thead>
<tr>
<th></th>
<th>AR32Z</th>
<th>MicroBlaze*</th>
</tr>
</thead>
<tbody>
<tr>
<td>LUT count</td>
<td>1,464</td>
<td>1,550</td>
</tr>
<tr>
<td>Dynamic Power</td>
<td>7 mW</td>
<td>31 mW</td>
</tr>
<tr>
<td>Total DMIPS</td>
<td>110</td>
<td>90</td>
</tr>
<tr>
<td>DMIPS/MHz</td>
<td>1.0</td>
<td>0.9</td>
</tr>
<tr>
<td>Board Current Consumption</td>
<td>187 mA</td>
<td>209 mA</td>
</tr>
</tbody>
</table>

* MicroBlaze Processor is generated for equivalent Microcontroller configuration.

77% less dynamic power than MicroBlaze
# AR32Z ASIC Implementation Results

## Used Configuration of AR32Z: RV32IM (Single-Cycle mult.) + Dynamic Branch Prediction

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process Node</td>
<td>TSMC 40nm LP</td>
</tr>
<tr>
<td>Std Library</td>
<td>Dolphin Tech. 6-track</td>
</tr>
<tr>
<td>Clock Frequency</td>
<td>350 MHz</td>
</tr>
<tr>
<td>Macro Dimension</td>
<td>121.8 um x 151.9 um</td>
</tr>
<tr>
<td>Std. Cells / Flipflops</td>
<td>11,369 / 1,685</td>
</tr>
<tr>
<td>Std. Cell utilization</td>
<td>82%</td>
</tr>
</tbody>
</table>

### Power Consumption:

<table>
<thead>
<tr>
<th></th>
<th>Leakage</th>
<th>Total Dynamic Power</th>
<th>Dynamic (uW/MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.953 mW</td>
<td>2.408 mW</td>
<td>6.879 uW/MHz</td>
</tr>
</tbody>
</table>

### Wire Length Statistics (mm):

<table>
<thead>
<tr>
<th>Layer</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>0.0544</td>
</tr>
<tr>
<td>M2</td>
<td>12.08</td>
</tr>
<tr>
<td>M3</td>
<td>42.05</td>
</tr>
<tr>
<td>M4</td>
<td>44.70</td>
</tr>
<tr>
<td>M5</td>
<td>49.39</td>
</tr>
<tr>
<td>M6</td>
<td>51.78</td>
</tr>
</tbody>
</table>
AR32Z feature as AI Accelerator

- Accelerator will be tightly coupled to the processor providing low latency interface.
- Accelerators can come from ASA or 3rd party developers.
- Accelerators can range from DSP to AI inferencing such as image processing, audio processing, DSP and many more.
ARSIM (C/C++ Based SoC simulation)

- **C/C++ Model Library**: Most of the required IPs for IoT/Edge SoC is part of this library including ASA RISC-V processor

- **RTL to C/C++ Conversion Engine**: ARSIM conversion engine can be used to convert the customer RTL into ARSIM C/C++ model for ARSIM verification

- **Verification Engine**: customer specific SoC can be dynamically built to create SoC for specific application using the IPs and bus fabrics as part of the ARSIM verification environment. Once the SoC is built, ARSIM enables customers to load the application C/C++ programs into the ARSIM to run the application specific programs to run the verification and analysis of the SoC system

- **RISC-V processor from other vendors can also be used**

Reduces design verification and design TAT by as much as 30%
ASA Processor / Products Road Map

2020-2023
Next exciting 3 Years for AI

2020
Q1
AR32Z
Low Power processor
Q2
Super-scaler processor
Q3
AR128V
Vector Processor for AI inferencing
Q4
XENON
FPGA Based SoC Products

2021
Q1
Q2
4 Processor Cluster
Quad-core Solutions
Q3
Q4
AR128V
Vector Processor for AI inferencing

2022
Q1
AR32/64AP
Application Processor running Linux
Q2
Vision Processor
Embedded Vision for Image Processing
Q3
Chiplet based Multicore
AI inferencing at Chiplet based Multi-core Solution
Q4

2023
ASA Edge AI Solutions

Custom Accelerator
- Tightly coupled with ASA Processor
- Low latency
- Low Power
- Complete FPGA solutions available

Vector Processor
- General Purpose accelerator for all AI/ML applications
- Low Power
- Highly software configurable
- FPGA/ASIC Solution

Multi-Core
- Heterogeneous low power chiplet based system design
- Highly configurable
- Rapid time-to-market
- Suitable for multiple AI/ML applications including 5G
ASA Engagement Objectives

● Seeking Strategic Partners to Accelerate ASA Business Success

● Key Elements of Partnership:
  ○ Product Development:
    ▪ Foundry support
    ▪ Packaging with emphasis on Chiplet technology
    ▪ Access to essential IP
    ▪ Development tools
Thank You