AI: scale from Edge to Server with RISC-V and Linux
What Age Are We In

**Agile Hardware Development**
Accelerate chip development and commercial adoption

**Improved Security**
Prevent side channel attack for example

**Open ISA**
Industry-standard open ISA

**Security**

**DSA**

**Domain-Specific Architectures**
Tailored to a specific problem domain and offer significant performance/efficiency gains

Source: https://www.acm.org/hennessy-patterson-turing-lecture
OPEN ISA RISC-V

- Open ISA inspired by the success of open source software - Linux for processors
- Greater competition drive quicker innovation
- Incredible ecosystem support
Active Roles in RISC-V International

Frankwell Lin, CEO
RISC-V
Board Member

Dr. Charlie Su, CTO
Vice Chair, Technical
Steering Committee

Florian Wohlrab
RISC-V
Ambassador
Tổng quát Andes

Who We Are

- Pure-play CPU IP Company
- RISC-V Founding Premier Member
- Taiwan Stock Exchange Listed

Quick Facts

- 15 years old company
- 200+ Licensees Worldwide
- 80% R&D employees
- 5B+ accumulated Andes-embedded SoC shipped
- 17K+ AndeSight IDE installation

Running Task Groups

Licensees Worldwide:
- USA
- France
- Beijing
- Korea
- Netherlands
- Israel
- Shanghai
- Japan
- Shenzhen
- Taiwan HQ

Taking RISC-V ® Mainstream
RISC-V
Market adoption and usage examples
RISC-V Momentum Changing Processor Landscape

General-Purpose/Applications

ARM Domination
- GP MCU
- Smartphone Processors
  - App Processors

RISC-V Stronghold
- House Keeping
- DSP
  - Vector Datapath

Deeply-Embedded
- Offload FSM

Performance-driven
- Cost-sensitive

- RISC-V business quickly started in:
  - Cost affordable
  - Replacement of FSM and house keeping

- RISC-V is catching up MCU but not phone and tablet yet

- Andes focuses on real-time & performance
  - Bringing accelerators closer to CPUs
  - AI/AR/VR/CV/etc. in-between layer work-load
  - Efficiently move data
Andes RISC-V on Audio product

- D25F on LE Audio (BLE 5.2) for True Wireless Earbuds and Hearing Aids
  - Customer Tape out already!

This product will be the one of the first SoCs supporting both of LE audio and Classic Audio

- Bluetooth Baseband and Audio Subsystem
  - LC3 codec - high quality, low power
  - LE Audio/BLE 5.2 – Multi-Stream, Broadcast Audio

- Application CPU
  - Power Efficient – Excellent PPA
  - Mature Ecosystem – Support various RTOSs
  - RISC-V DSP Extension – outstanding performance
  - DSP library

- DSP/AI Accelerator
  - DSP Algorithm for Noise and Echo Cancelation
  - Machine Learning for Key Word Spotting
Example of Edge Computing – Vision Processing

Pre-ISP Processing & Post Processing

Image Processing
Vector Processor
NX27V
VLEN=256b

NN Processing
Vector Processor
NX27V
VLEN=512b
Accelerator

ISP
Control Core
A25MP
DMA
SRAM
AXI BUS / NOC
DDR Interface
Other I/O
ISP Interface

Legend:
- Andes
- Third Party
Example of Cloud Computing - Datacenter

Data Processing
- Main CPU Multicore AX27MP/45MP
- Vector Processor NX27V

Legend:
- Blue: Andes
- Gray: Third Party

SRAM

NN Processing
- Coordinator Core A27
- Controller NX27V
- Accelerator

PCIx Interface
DDR Interface
RISC-V
Added Value and contributed extensions
Andes Added Value in RISC-V

- Andes extensions to RISC-V
  - Baseline ISA extension to speed up memory access and branches
  - CoDense to reduce code size (12% better measured by GCC)
  - PowerBrake to save power by stalling pipeline
  - StackSafe HW stack protection
  - vPLIC vectored dispatch and preemption (reduce 57% of latency)

- Powerful features to differentiate your products
- Create competitive edge for your systems
• Andes contributed market-proven DSP(SIMD) as P-Extension
• Designed to accelerate slow video, audio/voice and low data rate DSP workloads

Real world speedup using P-Extension

- MP3 decode: 2 times speedup
- AMR voice codec: 3.7 times speedup
- ML-KWS (keyword spotting): 5.2 times speedup
- PNET (90% of Face Detection): 8.9 times speedup
- CIFAR10 (Image Classification): 14 times speedup

Increase power efficiency to your DSP applications
Andes Custom Extension – EDA Tool

- ACE unlocks RISC-V’s Potential of RISC-V DSA
  - Define ACE instructions to handle time critical codes
  - Another approach to co-processor or accelerators

- All-in-one COPILOT development environment
  - EDA Automation tool and ease of use
  - Extensions are easy to re-use, can be used as a library
AndesCore™ RISC-V Families

Features/Performance

- **N(X)45**: V5, Dual Issue, Superscalar, FPU, PMP
- **D(X)45**: N(X)45, FPU, DSP
- **A(X)45**: D45, MMU
- **A(X)45MP**: L2$, L1/IO coherence
- **NX27V**: 5-stage CPU, 128/256/512b data width VPU
- **D25F**: N25F, DSP
- **A(X)25**: N(X)25F, MMU, DSP
- **A(X)25MP**: L2$, L1/IO coherence
- **N(X)25F**: V5/32&64b, FPU, PMP
- **A(X)27**: MemBoost, MMU, DSP
- **A(X)27MP**: MemBoost, L2$, L1/IO coherence
- **N22**: V5[e], 32/16 GPR

- **8-stage 1.2GHz**: A(X)45MP
- **5-stage 1.1GHz**: A(X)25MP
- **2-stage 700MHz**: N22

- **Fast and Compact /Slim and Efficient**
- **DSP Extension**
- **Linux with FPU/DSP**
- **Cache-Coherent Multicores**

In Production: 
- **N(X)45**: V5, Dual Issue, Superscalar, FPU, PMP
- **D(X)45**: N(X)45, FPU, DSP
- **A(X)45**: D45, MMU
- **A(X)27**: MemBoost, MMU, DSP
- **N(X)25F**: V5/32&64b, FPU, PMP
- **A(X)25**: N(X)25F, MMU, DSP
- **A(X)25MP**: L2$, L1/IO coherence
- **N22**: V5[e], 32/16 GPR

In Development: 
- **NX27V**: 5-stage CPU, 128/256/512b data width VPU
- **D25F**: N25F, DSP
- **A(X)45MP**: L2$, L1/IO coherence
- **A(X)27MP**: MemBoost, L2$, L1/IO coherence

*: TSMC 28HPC+ RVT, SS, 0.81V, 0C, with I/O constraints.
V-Series
Cray style, scalable vector processor
First RISC-V Vector Engine Shipped in Industry!

RVV v0.8 support*
AI optimized with BFloat16 & INT4
1GHz, 0.3mm² in TSMC 7nm FF+

Configurable & scalable
- Vector length 128-bits to 512-bits
- Licensee configurable ALUs

Low power, simple to use
- Multi-level clock-gating
- In-order, 1R/W SRAM, cell based

> 50 VPU in < 10W Open Compute card
Core Overview

Some details

From 2-stage over 5-stage to 8-stage
AndesCore™ 25 Series

- 32-bit and 64-bit cores
- AndeStar V5 architecture:
  - RV-IMACF + Andes V5 Extensions
  - Optional: F/D and S-mode/MMU
- 5-stage pipeline, single-issue
- Configurable multiplier
- Optional branch prediction
- I/D caches and Local Memory:
  - Optional parity or ECC protection
  - Hit-under-miss caches
  - HW unaligned load/store accesses
- Bus interface:
  - A master port (AHB, AXI, AXIx2)
  - An optional slave port (AHB)

AndesCore™ A25MP/A2X2MP Multicore

- 1~4 A25/A2X2 CPUs:
  - RV-IMACF ISA + V5 extensions
  - P-extension draft
  - Supporting SMP Linux

Bus Interfaces
- LM slave port
- Coherence slave port
- AXI bus master interface
- N:1 synchronous clock ratio

PLIC for interrupt handling
- Debug/trace support
- Andes Coherence Unit
  - MESI cache coherence protocol
  - Duplicate L1 dcache tags
  - IO coherence for cacheless masters
  - L2 Controller
  - Size: 128KB to 2MB
AndesCore™ 45 Series

- **8-stage in-order dual-issue**
- **AndeStar™ V5 ISA:**
  - RV*GCN (S/D FPU)
  - RV*P-ext (DSP/SIMD)
  - MMU: for Linux Applications
  - ALL have Andes extensions
- **Dual-issue most instruction pairs**
  - Except for 2 MUL/FPU/DSP/LD_ST and some special dependent ALU instruction pairs
  - Late ALUs enable 0-cycle load-use penalty
- **MemBoost** for memory subsystem
- **Low power dynamic branch prediction**
- **Unaligned data accesses**
- **Fast or small multiplier**

F1 F2 ID II EX MM LX WB

<table>
<thead>
<tr>
<th>ALU0</th>
<th>ALU1</th>
<th>ALU2</th>
<th>ALU3</th>
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<td>I$/ILM</td>
<td>DEC</td>
<td>ISS</td>
<td>AG</td>
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- **Multiplier**
- **DSP**
- **Floating Point Unit**

($)LM: 2nd cycle for alignment

45-Series Pipeline
Time-to-Market

Get the whole set, IDE, Debug Probes, BSP’s and Core IP
Complete Development Environment

- **AndeSight™ Feature-Rich IDE**
  Free Evaluation on SID and ICE target

- **AndeShape™ Development Boards**
  Full-Featured ADP-XC7K
  Corvette-F1 Amazon FreeRTOS-qualified

- **AndeSoft™ Software Stack**
  Bare metal demo projects
  FreeRTOS ver10
  Linux

- **Debugging Hardware**
  AICE-MINI+, AICE-MICRO
IAR Embedded Workbench®
- Support RISC-V
- Support P-Extension (DSP/Packed-SIMD)
- Excellent optimization technology
- Static code analysis
- Extensive Debugging via I-jet probe
Root-of-Trust Solution

- FIPS-140-2 Level 2 certified
- Secure Boot
- Side Channel Protection
- Anti-Tampering
- HW Protection for Keys
- TLS Device Authentication
- Secure DMA
- Secure Debug

Crypto data plane
- AES
- SHA2
- ...
- ECC
- TRNG

Secure Storage for Keys (OTP, PUF)

Secure Debug Ctrl

Controller

System Bus (AXI, AHB, APB)

Slave I/F

Master I/F

Secure mbox

Secure DMA

RAM

TCM I/F

Secure Debug Ctrl

CoProc I/F

Controller

Prog. Mem

Data RAM

Timers

Secure I/O

Secure Storage for Keys (OTP, PUF)
Summary

• RISC-V has built a strong ecosystem contributing technologies and innovations
• RISC-V keeps evolving through the collaborative community
• Andes is the only ONE provides P & V & custom extension framework to accelerate AI
• Commercialization, customization and user experience will be the three keys to succeed

JOIN RISC-V!
WORK WITH ANDES!
Cảm ơn bạn

THANK YOU